This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended): A delay circuit comprising:

a clocked inverter circuit to which a first pulse signal is supplied, said clocked inverter circuit being controlled by the first pulse signal to output~~outputting~~ a second pulse signal having one of a first pulse width and a second pulse width, the first pulse width being greater than a pulse width of the first pulse signal and the second pulse width being smaller than the pulse width of the first pulse signal; and

a logic circuit to which the second pulse signal output from the clocked inverter circuit and an inverted signal of said first pulse signal are supplied, wherein said logic circuit outputs a third pulse signal, the third pulse signal having the other one of the first pulse width and the second pulse width.

Claim 2 (original): The delay circuit according to claim 1, wherein said logic circuit is a NOR circuit and said clocked inverter circuit delays a trailing edge of said third pulse signal.

Claim 3 (original): The delay circuit according to claim 1, wherein said logic circuit is a NAND circuit and said clocked inverter circuit delays a leading edge of said third pulse signal.

Claim 4 (original): The delay circuit according to claim 1, wherein said clocked inverter circuit is composed of an NMOS transistor and a PMOS transistor and at least one of a channel width, channel length, threshold voltage, and substrate voltage of the NMOS is different from a channel width, channel length, threshold voltage, and substrate voltage of the PMOS transistors.

Claim 5 (original): The delay circuit according to claim 4, wherein a ratio of a current driving capability of said PMOS transistor to a current driving capability of said NMOS transistor is set to a value other than one and a rise time of a pulse signal is made different from a decay time of the pulse signal.

Claim 6 (previously amended): A delay circuit comprising:

an inverter circuit controlled by a clock signal to which a first pulse signal is supplied, said inverter circuit outputting a second pulse signal having one of a first pulse width and a second pulse width, the first pulse width being greater than a pulse width of the first pulse signal and the second pulse width being smaller than the pulse width of the first pulse signal; and

a logic circuit to which the second pulse signal output from the inverter circuit and the inverted signal of said first pulse signal are supplied, wherein said logic circuit outputs a third pulse signal, the third pulse signal having the other one of the first pulse width and the second pulse width.

Claim 7 (previously added): The delay circuit according to claim 6, wherein said logic circuit is a NOR circuit and said inverter circuit delays a trailing edge of said third pulse signal.

Claim 8 (previously added): The delay circuit according to claim 6, wherein said logic circuit is a NAND circuit and said inverter circuit delays a leading edge of said third pulse signal.

Claim 9 (previously added): The delay circuit according to claim 6, wherein said inverter circuit is composed of an NMOS transistor and a PMOS transistor, and at least one of a channel width, channel length, threshold voltage and substrate voltage of the NMOS transistor is different from a channel width, channel length, threshold voltage and substrate voltage of the PMOS transistor.

Claim 10 (previously added): The delay circuit according to claim 9, wherein a ratio of a current driving capability of said PMOS transistor to a current driving capability of said NMOS transistor is set at a value other than one and a rise time of said first pulse signal is made different from the decay time of said first pulse signal.

Claim 11 (previously amended): A delay circuit applied to a synchronizing circuit comprising:

a first delay line which includes unit delay elements and transfers a forward pulse signal;

a second delay line which includes unit delay elements and transfers a backward pulse signal; and

a state holding section which is brought into a set state or a reset state according to a transfer position of the forward pulse signal transferred along said first delay line and said backward pulse signal transferred along said second delay line in the set state and a clock signal along said second delay line in the reset state,

wherein each of said unit delay elements constituting said first and second delay lines includes:

a clocked inverter circuit to which a first pulse signal corresponding to one of said forward and backward pulse signals output from a preceding delay unit is supplied, said clocked inverter circuit outputting a second pulse signal having one of a first pulse width and a second pulse width, the first pulse width being greater than a pulse width of the first pulse signal and the second pulse width being smaller than the pulse width of the first pulse signal; and

a logic circuit to which the second pulse signal output from the clocked inverter circuit and an inverted signal of said first pulse signal are supplied, wherein said logic circuit outputs a third pulse signal, the third pulse signal having the other one of the first pulse width and the second pulse width.

Claim 12 (previously added): The delay circuit according to claim 11, wherein said logic circuit is a NOR circuit and said clocked inverter circuit delays a trailing edge of said first pulse signal.

Claim 13 (previously added): The delay circuit according to claim 11, wherein said logic circuit is a NAND circuit and said clocked inverter circuit delays a leading edge of said first pulse signal.

Claim 14 (previously added): The delay circuit according to claim 11, wherein said clocked inverter circuit is composed of an NMOS transistor and a PMOS transistor, and at least one of a channel width, channel length, threshold voltage and substrate voltage of the NMOS transistor is different from a channel width, channel length, threshold voltage and substrate voltage of the PMOS transistor.

Claim 15 (previously added): The delay circuit according to claim 14, wherein a ratio of a current driving capability of said PMOS transistor to a current driving capability of said NMOS transistor is set at a value other than one and a rise time of said first pulse signal is made different from the decay time of said first pulse signal.

Claim 16 (currently amended): A delay circuit comprising:

a clocked inverter circuit to which a first pulse signal is supplied, said clocked inverter circuit being controlled by the first pulse signal to output~~outputting~~ a second pulse signal having a pulse width wider than a pulse width of the first pulse signal; and

a logic circuit to which the second pulse signal output from the clocked inverter circuit and an inverted signal of the first pulse signal are supplied, wherein said logic circuit outputs a third pulse signal, the third pulse signal having a pulse width narrower than the pulse width of the second pulse signal and equal to the pulse width of the first pulse signal.

Claim 17 (currently amended): A delay circuit comprising:

a clocked inverter circuit to which a first pulse signal is supplied, said clocked inverter circuit being controlled by the first pulse signal to output~~outputting~~ a second pulse signal having a pulse width narrower than a pulse width of the first pulse signal; and

a logic circuit to which the second pulse signal output from the clocked inverter circuit and an inverted signal of the first pulse signal are supplied, wherein said logic circuit outputs a third pulse signal, the third pulse signal having a pulse width wider than the pulse width of the second pulse signal and equal to the pulse width of the first pulse signal.

Claim 18 (new): A delay circuit comprising:

a first delay element; and

a second delay element connected in series to the first delay element,

the first delay element including

a first clocked inverter circuit to which a first pulse signal is supplied, said first clocked inverter circuit outputting a second pulse signal having one of a first pulse width and a second

pulse width, the first pulse width being wider than a pulse width of the first pulse signal and the second pulse width being narrower than the pulse width of the first pulse signal; and

a first logic circuit to which the second pulse signal output from the first clocked inverter circuit and the inverted signal of said first pulse signal are supplied, wherein said first logic circuit outputs a third pulse signal, the third pulse signal having another one of the first pulse width and the second pulse width,

the second delay element including

a second clocked inverter circuit to which the third pulse signal is supplied, said second clocked inverter circuit outputting a fourth pulse signal having one of the first pulse width and the second pulse width, the first pulse width being wider than a pulse width of the third pulse signal and the second pulse width being narrower than the pulse width of the third pulse signal; and

a second logic circuit to which the fourth pulse signal output from the second clocked inverter circuit and said second pulse signal are supplied, wherein said second logic circuit outputs a fifth pulse signal, the fifth pulse signal having another one of the first pulse width and the second pulse width.

Claim 19 (new): A delay circuit comprising:

a first delay element; and

a second delay element connected in series to the first delay element,

the first delay element including

a first inverter circuit controlled by a clock signal to which a first pulse signal is supplied, said first inverter circuit outputting a second pulse signal having one of a first pulse width and a second pulse width, the first pulse width being wider than a pulse width of the first pulse signal and the second pulse width being narrower than the pulse width of the first pulse signal; and

a first logic circuit to which the second pulse signal output from the first inverter circuit and said first pulse signal are supplied, wherein said first logic circuit outputs a third pulse signal, the third pulse signal having another one of the first pulse width and the second pulse width,

the second delay element including

a second inverter circuit controlled by a clock signal to which the third pulse signal is supplied, said second inverter circuit outputting a fourth pulse signal having one of the first pulse width and the second pulse width, the first pulse width being wider than a pulse width of the third pulse signal and the second pulse width being narrower than the pulse width of the third pulse signal; and

a second logic circuit to which the fourth pulse signal output from the second inverter circuit and said second pulse signal are supplied, wherein said second logic circuit outputs a fifth pulse signal, the fifth pulse signal having another one of the first pulse width and the second pulse width.

20. (new): A delay circuit comprising:

a clocked inverter circuit to which a first pulse signal is supplied, said clocked inverter circuit outputting a second pulse signal having one of a first pulse width and a second pulse width in response to the first pulse signal only, the first pulse width being greater than a pulse width of the first pulse signal and the second pulse width being smaller than the pulse width of the first pulse signal; and

a logic circuit to which the second pulse signal output from the clocked inverter circuit and an inverted signal of said first pulse signal are supplied, wherein said logic circuit outputs a third pulse signal, the third pulse signal having the other one of the first pulse width and the second pulse width.